Remarks

Entry of the foregoing amendment is believed to place the application in condition for allowance.

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-6, 9, 10, 14-16, 18-26 are pending in the application, with claims 1 and 14 being the independent claims. Claims 11 and 13 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 11 and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by Ohara et al. (US Patent 5,694,588 "Ohara").

Although the Applicants respectfully disagree with the Examiner's rejections of previously presented claims 11 and 13, the Applicants have canceled claims 11 and 13 to expedite prosecution. Thus, the Examiner's previous rejections with respect to claims 11 and 13 are moot in light of the current Amendment.

Rejections under 35 U.S.C. § 103

Claims 1-6, 9, 10, 14-16, and 18-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ohara in view of Kori (U.S. Patent No. 6,035,094 "Kori"). Applicants respectfully traverse.

Claim 1 describes "a timing generator" comprising the element "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory." The combination of Ohara and Kora does not disclose this element.

The plain meaning of the word "plurality" implies more than one. Further, from the plain language of claim 1, a microsequencer is at least something that produces a flag based on a program stored in a random access memory. Thus, to anticpate the element "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory," a reference must disclose more than one microsequencers that produce a flag based on a program stored in a random access memory.

In the Office Action dated August 31, 2007, the Examiner relies on Col. 4 lines 16-26 and Col. 12 lines 36-60 of Ohara as allegedly teaching "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory." Col. 4 lines 16-26 of Ohara states:

> In a typical application, such as video signal processing, the Input and Output layers operate in synchronism with the data source (such as video camera, VCR, receiver, etc.) and the data sink respectively (such as the raster display). Concurrently, the Computation layer performs the desired transformation by the application of programmable functions simultaneously to all the elements of a packet (commonly referred to as a VECTOR: within the TV/Video environment all the samples comprising a single horizontal display line). Thus the SVP is architecturally streamlined for Synchronous Vector Processing.

This passage does not disclose a "microsequencer" that produces a flag based on a program stored in a random access memory, let alone, "a plurality of

microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory."

Col. 12 lines 36-60 of Ohara provides a description of Instruction Generator 334 shown in Fig. 14. Ohara describes Instruction Generator 334 as feeding SVP 102 of Fig. 1. See Col. 13 lines 33-47. Regardless of whether the Instruction Generator 334 is equivalent to the claimed "microsequencer," for at least the reason that Ohara does not disclose where there are more than one Instruction Generators, Ohara does not disclose "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory." Ohara consistently discloses a single Instruction Generator feeding SVP 102. See e.g. Fig. 1 and Col. 5 lines 4-21. Kori does not make up for the deficiencies of Ohara.

For at least the reason that the combination of Ohara and Kori does not disclose "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory," claim 1 is patentable over the combination of Ohara and Kori.

Independent of the fact that the combination of Ohara and Kori does not disclose "a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory," claim 1 is patentable of the combination of Ohara and Kori for at least the alternative reason that the combination of Ohara and Kori does not disclose "a timing generator" comprising "a programmable combinational logic module, coupled to said plurality of microsequencers that generates control signals based on the flags produced by said plurality of microsequencers to support a copy protection process."

In the Office Action dated August 31, 2007, the Examiner relies Col. 13 lines 33-47 of Ohara as allegedly teaching "a programmable combinational logic module, coupled to said plurality of microsequencers that generates control signals based on the flags produced by said plurality of microsequencers to support a copy protection process." It appears as though the Examiner is relying on SVP core processor 102 anticipating "a programmable combinational logic module...that generates control signals." Col. 13 lines 33-47 of Ohara does not describe where SVP core processor 102 generates control signals. Further, description of SVP core processor 102 throughout Ohara is consistently describes the SVP core processor 102 as simply providing processed digital signals and does not describe the SVP core processor as producing control signals. See e.g. Col. 4 line 45-47.

FIG. 4 of the present application provides an exemplary embodiment of a programmable combinational logic module. It should be noted that this exemplary embodiment of a programmable combinational logic is consistent with "combinational logic" as a term of art which is distinct from the term of art, "sequential logic." SVP core processor 102 is not consistent with "combinational logic" as a term of art. Kori does not make up for the deficiencies of Ohara.

For at least the reason that the combination of Ohara and Kori does not disclose "a programmable combinational logic module, coupled to said plurality of microsequencers that generates control signals based on the flags produced by said plurality of microsequencers to support a copy protection process," claim 1 is patentable over the combination of Ohara and Kori.

Claims 2-6, 9 and 10 each depend on independent claim 1 discussed above. Thus, for at least the reasons discussed above, they are also allowable over the combination of Ohara and Kori. Reconsideration and allowance of claims 2-6, 9 and 10 are respectfully requested.

Claim 14 includes the element "executing a set of programs from said plurality of programs by a plurality of microsequencers to generate a set of flags." The combination of Ohara and Kora do not disclose this element because the combination of Ohara and Kora does not disclose "a plurality of mircosequencers" for at least the reasons stated above. Because the combination of Ohara and Kora does not disclose "executing a set of programs from said plurality of programs by a plurality of microsequencers to generate a set of flags" claim 14 is patentable of the combination of Ohara and Kora.

Claims 15-16 and 18-26 each depend on independent claim 14 discussed above. Thus, for at least the reasons discussed above, they are also allowable over the combination of Ohara and Kori. Reconsideration and allowance of claims 15-16 and 18-26 are respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason,

that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael D. Specht
Attorney for Applicants
Registration No. 54,463

Date: 1/30/08

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
719297_1.DOC